If ARPA project, please check below:

INVENTION DISCLOSURE

___ Advanced SRAM
___ BST
___ FED
___ FE RAM
___ NCAICM

1. INVENTOR(S): Fernando Gonzalez

Chandra Mouli

2. DESCRIPTION

2.1 Title of invention:

A Novel Raised Source Drain Structure utilizing a Pocket Junction

2.2 Brief description:
The prior art uses a thin film to isolate the Raised Source-Drain from the poly gate.This is a disadvanatge for capacitance loading. Also, the prior art uses a n- implanted region under the Raised Source Drain . The present disclosure uses processing that outdiffuses dopant from the poly into the Source-drain to form a ultra shallow N- region. A N+(P+) pocket is formed by implanting through the thin gap space that forms a new transistor structure. The poly films are implanted through a thin conductive film (Ti) to prevent the gates from damage. However, the Ti is removed from the nitride spacer area so that the air gap can be created.

2.3 Also attach a complete description, including drawings or sketches and articles relevant to the invention. Legible photocopies of laboratory notebooks are acceptable.

3. INFORMATION CONCERNING CONCEPTION OF INVENTION

3.1 CONCEPTION AND DOCUMENTATION OF THE INVENTION

a. Identify the date when you first conceived the invention. (If not sure, give the earliest date of which you are sure.)

b. To whom was the idea first described and on what date? (Other than a co-inventor.)
Mike Violette

c. Identify the date of the first tangible record such as computer simulation, tape out, drawing or written description. Please specify type and location.
disclosure

3.2 CONCEPTION OF THE INVENTION

a. Please identify related invention disclosures, patents or other publications describing similar ideas, and other companies working in the same field. Attach copies, if available.
REgular Raised Source-DRains

b. What is the closest technology, of which you are aware?
UT Al Tasch's papers on Raised Source-Drains

c. Identify the advantages of this invention over previous technology.

1. redu. J masks
2. improved series resistance
3. CMOS integratable
4. surface channel pch device
5. nch has better drive with excellent punchthrough
6. Sidewall Capacitance is reduced.

3.3 IMPORTANT DATES

a. Has the invention been disclosed outside the company? NO. If yes, to whom, when, and in what form?

b. Have any articles describing your invention been published? No. If yes, list author(s), title of article, publication and date.

c. Have any engineering samples been given out? No.. If yes, to whom and on what date?

d. Has any product using the invention been sold or offered for sale? No.. If yes, to whom and on what date?

3.4 DISPOSITION OF THE INVENTION

a. When will (or did) Micron begin use of the invention experimentally?
Do not know.

b. When will (or did) Micron begin production of this invention?
Do not know.

3.5 MISCELLANEOUS INFORMATION

a. Was the invention developed during a joint development agreement or other contract with an outside company? None...

b. Please list developmental work outside of the company None... (including Government proposal or contract).

4. INVENTORS:

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Supervisor: Brent Gilgen

Signature: _____ Date: _____

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Micron Phone: 368-2092 Micron Mail Stop: 306

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_X_ Micron Technology, Inc. Dept. #: _____

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Supervisor: Joe Karniewicz

Signature: _____ Date: _____

-- If more than three inventors use additional form(s) available in the Legal Department, 3rd floor, Administration building. --

5. WITNESS

If there is only one inventor, a witness should sign and date this disclosure. A witness in this case is a non-inventor who understands the nature of the invention.

_____ _____
(Signature of Witness) (Date)

Note: If you have any questions or wish assistance completing this form, please call the Legal/Patent Department, ext. 4527.

A Novel Raised Source Drain Structure utilizing a Pocket Junction

Abstract:

Main interest in this disclosure lies in the ability to improve the sidewall decoupling of the raised source-drain to the poly gate; to connect the source-drains to the pocket junction next to the gate edge with a high dose implant for reduced series resistance, and to reduce the process flow to make both N+ and P+ poly and pocket junction by implantation. Also, the n- (p-) under poly can be outdiffused to shallow depth. Also, the blanket N+ pocket implant reaches the pchannel pocket but is countered doped by the P+ pocket implant. The excess phosphorous acts as a pchannel punchthrough halo.

Claims:

1. the gap opening thru which the N+ or P+ pocket implant is done.
2. the gap reduces the capacitance between gate and source-drain
3. method for N+ and P+ poly formation in combination with pocket formation

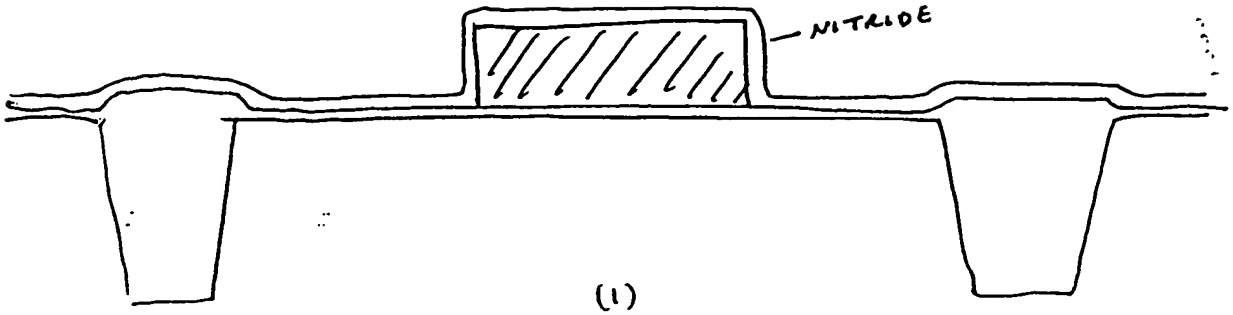
Process Description:

Fig. 1 shows the gate formation with a thin nitride film.
Fig. 2 shows the nitride spacer which forms the gap.
Fig. 3 shows the gate oxide removed from the S/D region and lightly n-type poly si deposited..
Fig. 4 shows the cmp of the poly.
Fig. 5 shows the S_D region patterning.
Fig. 6 shows the conductive layer and masking and implants n+ (p+) region.
Fig. 7 shows the gap etch and pocket implant.
Fig. 8 shows a non-conformal film to clsoe the top of the gap and insulating film.
Fig. 9 shows the contacts and metalization.

Process Flow:

- gate oxide
- poly gate dep and patterning
- nitride dep
- spacer etch
- oxide etch
- poly dep
- cmp
- pattern source-drain regions
- conductive layer
- N+ mask
- N+ implant
- P+ mask
- P+ implant
- Titanium mask
- titanium etch → NITRIDE ETCH
- N+ pocket implant
- P+ mask
- P+ pocket implant
- RTP sinter
- TiN etch
- RTP Anneal
- non-conformal oxide dep
- BPSG dep
- CMP
- Contact patterning
- contact plug formation
- metal dep

- metal patternin



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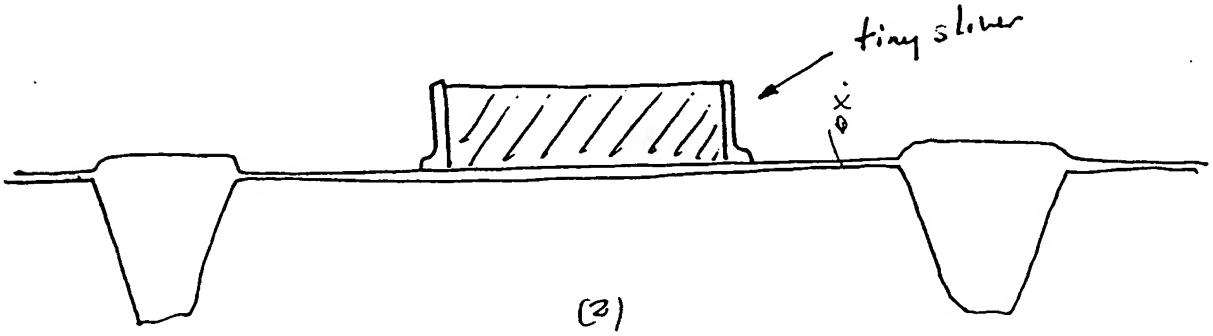

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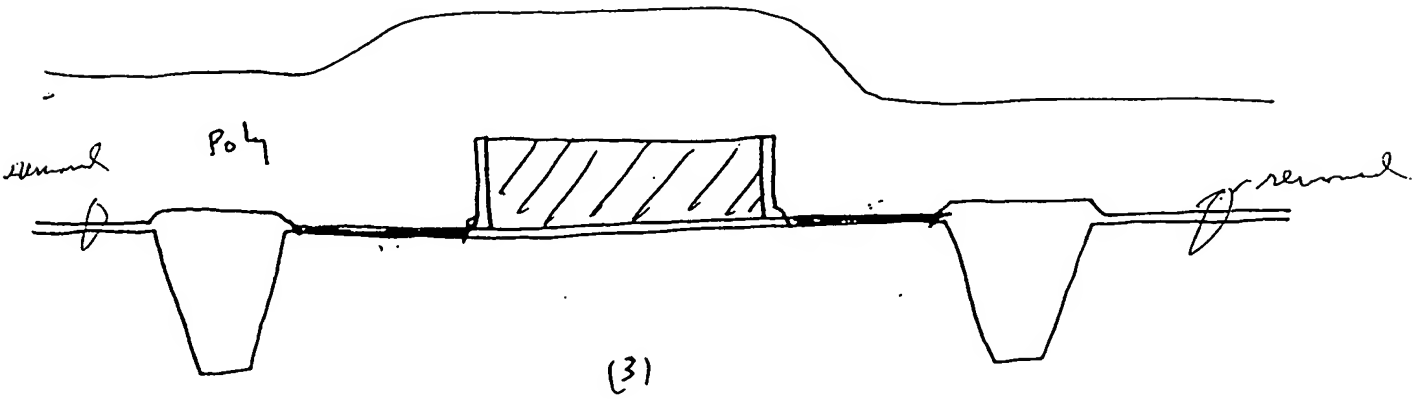

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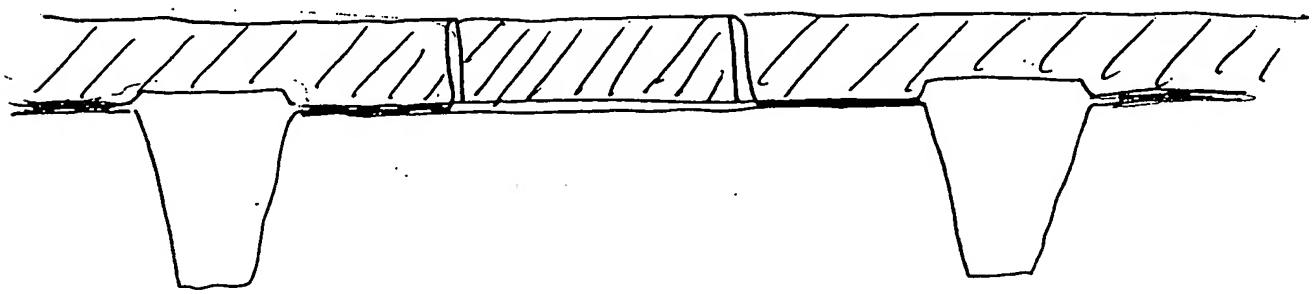

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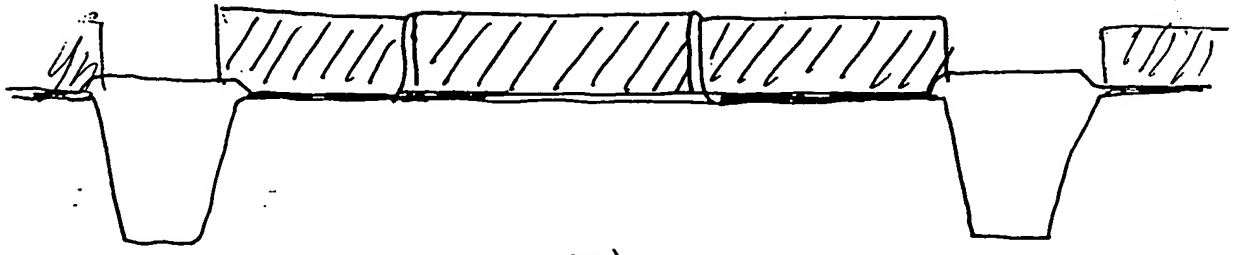

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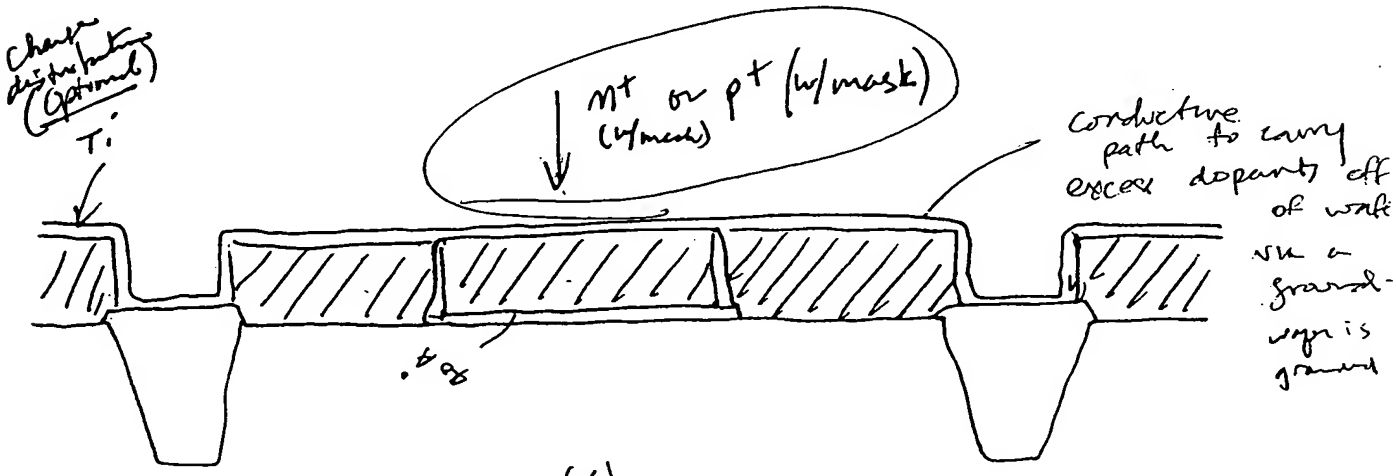

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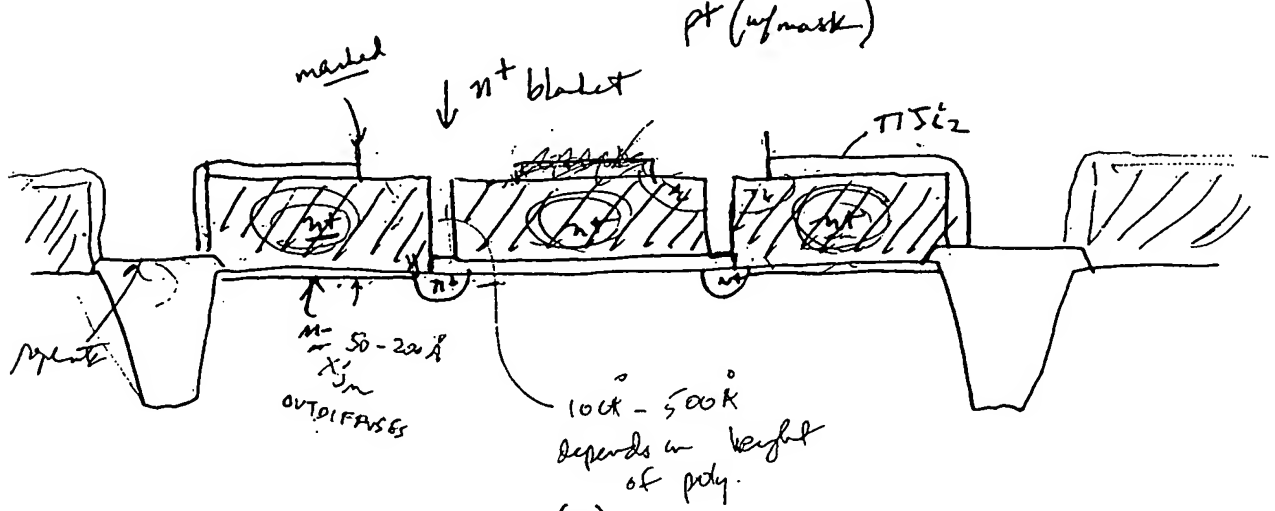

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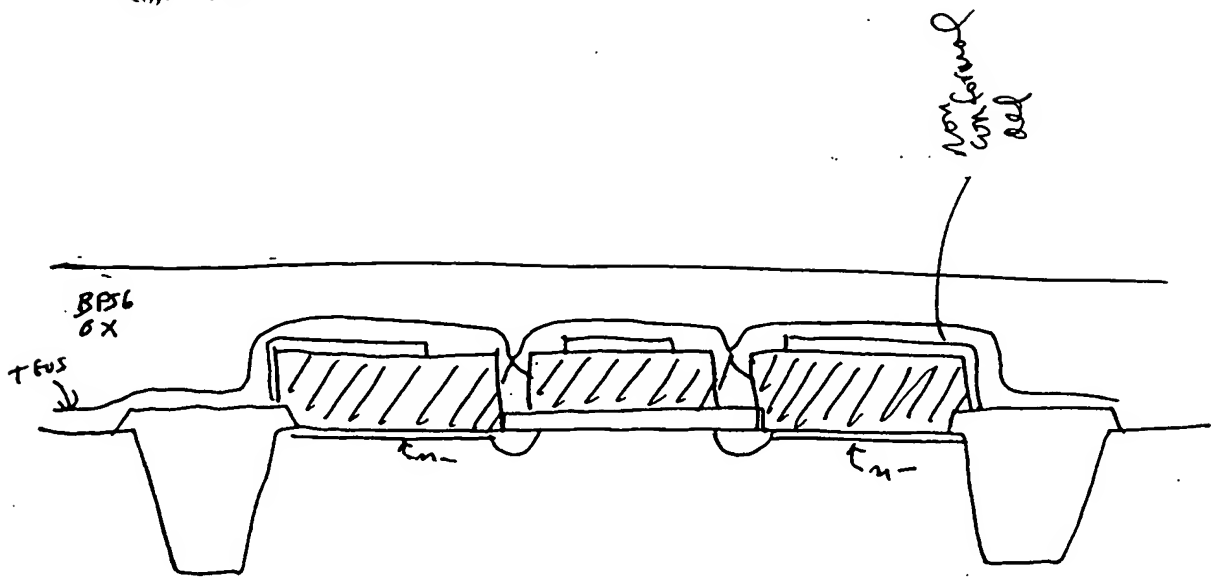

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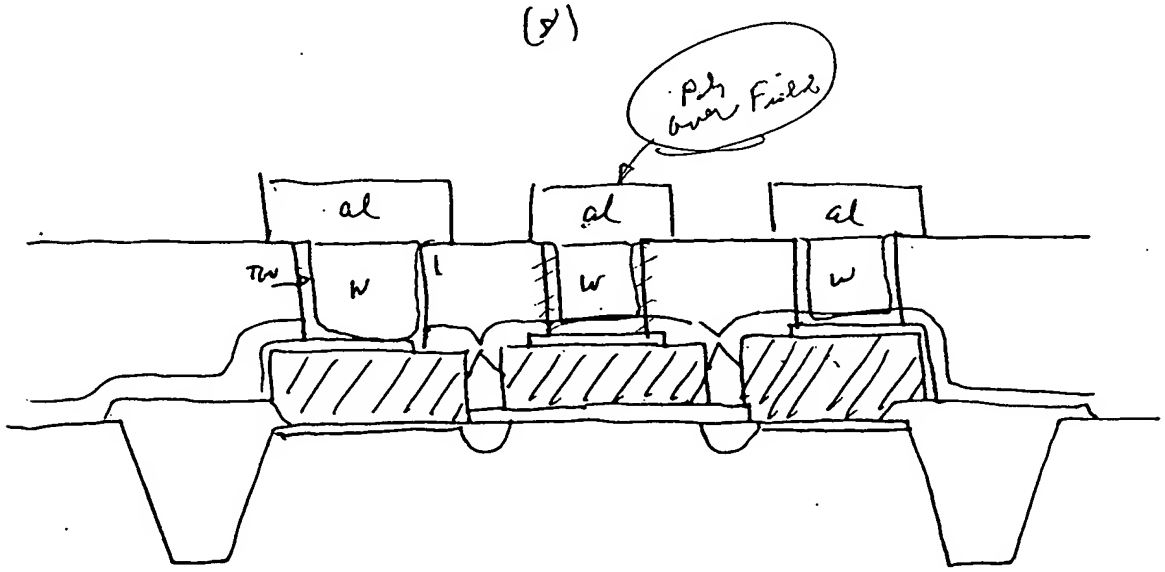

(b)

Gonzalez/Mouli

Novel Raised S/D structure utilizing pocket junction

File:

Prior art search done by Charles. Nothing found that leaves air gap spacers. Committee wanted to file if nothing in this area existed.

But be sure to emphasize the formation of the air spacer during disclosure

REFERENCE CHARACTER LIST FOR CASE

00		34	air gaps	67			
01		35		68			
02		36	pocket [illegible]	69			
03		37		70			
04		38	[illegible]	71			
05		39		72			
06		40	nonconformal layer	73			
07		41		74			
08		42	[illegible]	75			
09		43		76			
10	[illegible]	44	[illegible]	77			
11		45	adhesion layer	78			
12	[illegible]	46	[illegible]	79			
13		47		80			
14	OX layer	48	[illegible]	81			
15		49		82			
16	[illegible]	50	Seed	83			
17		51		84			
18	[illegible]	52	memory controller	85			
19		53		86			
20	[illegible]	54	RAM	87			
21		55		88			
22	Sacrificial layer	56	Bus	89			
23		57		90			
24	Spacer area	58	Processor	91			
25		59		92			
26	[illegible]	60	Bus	93			
27		61		94			
28	~~Pad~~ [illegible]	62	[illegible]	95			
29		63		96			
30	~~Pad~~ [illegible]	64	[illegible]	97			
31		65		98			
32	conductive layer	66	Storage device	99			
33							

Use to eliminate duplication of reference characters.